MEMTECH

VAYU X8808

AI-driven Memory Accelerator — CXL™ Type 3 Memory Expander

Up to 1 TB of DDR4 / LPDDR4 / LPDDR4X behind a PCIe® Gen5 ×16 / CXL 3.0 link, shared by up to 4 hosts with no switch — managed end-to-end by MII, MEMTECH's Memory Intelligence Infrastructure.

1 TB	4	4 hosts	< 350 ns	< 15 W
DDR4 / LPDDR4X behind one device	combo channels · DDR4-3200 / LPDDR4X-4266	×16 → 4××4 bifurcation, SRIS, no switch	added load-to-use latency (target)	controller power (target)

WHY X8808

Memory is the largest, least-observable line item in the data center. The X8808 expands it **and** makes it intelligent: an on-chip **Memory AI Agent** watches every channel's margins, temperature, errors and traffic in real time, predicts failures before they take a node down, retires weak pages proactively, and tunes cache, refresh and power autonomously — inside a hardware safety envelope, with every action reversible.

> **MII — Memory Intelligence Infrastructure.** A Layer 0–6 stack from DRAM physics to fleet learning. X8808 executes L3 (Memory AI Agent) and L4 (telemetry) in silicon and feeds L5 optimization / yield analytics and L6 cross-deployment learning — turning every deployed device into a sensor for the fleet.

KEY FEATURES

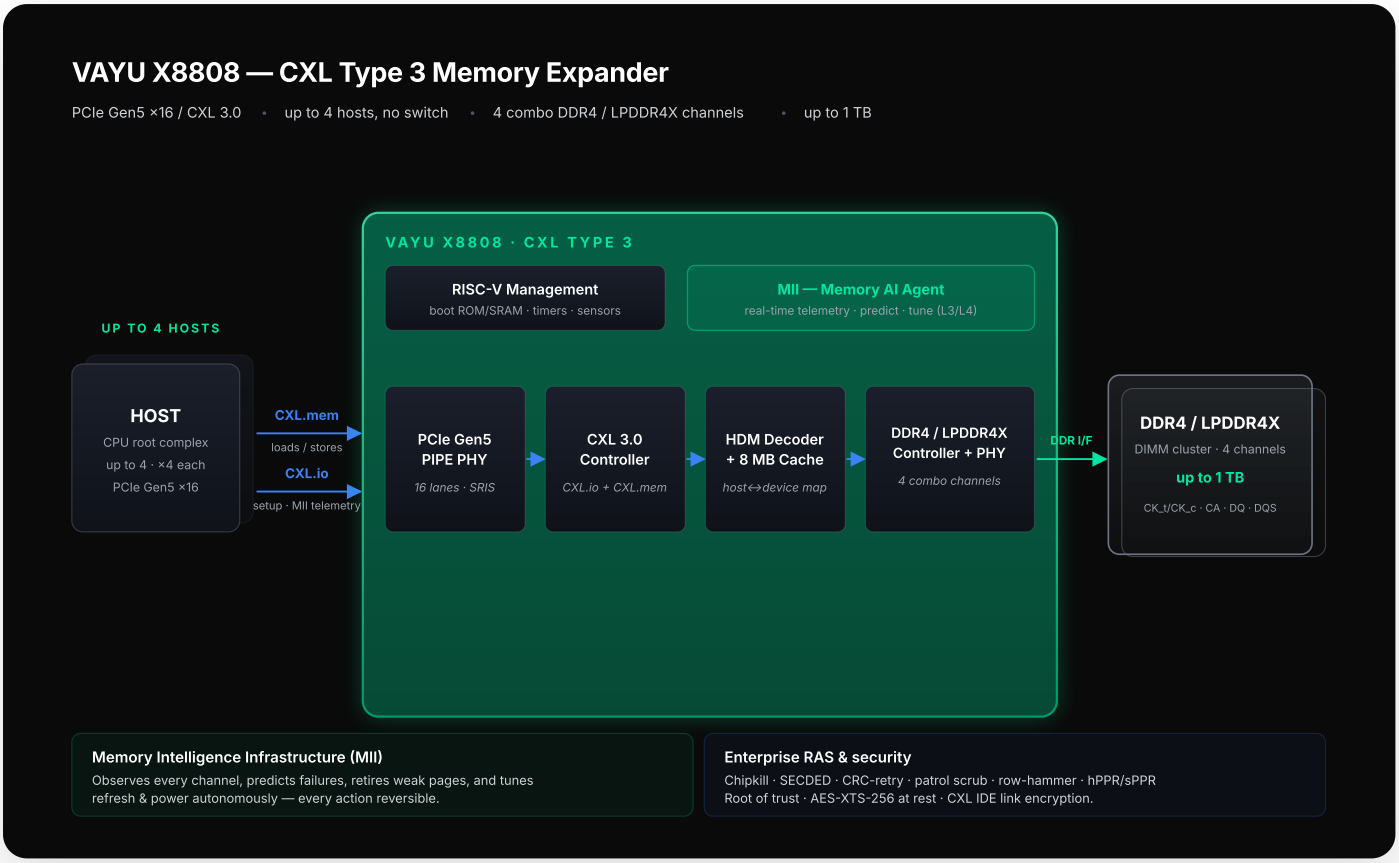
- CXL 3.0 (CXL.io + CXL.mem), backward compatible to 2.0 / 1.1; 68 B & 256 B flits
- PCIe Gen5 ×16 architecture; 16 GT/s first silicon, 32 GT/s PHY in evaluation
- 4 combo channels: DDR4-3200 72-bit 2 DPC · LPDDR4 / 4X to 4266 MT/s
- 8 MB MII-managed device cache; HDM interleave 1 / 2 / 4-way
- RAS: RS Chipkill, SECDED, CRC + retry, CA parity, scrub, row-hammer, hPPR / sPPR
- Security: root of trust, secure boot, AES-XTS-256 at rest, CXL IDE + SPDM on the link
- Standard Linux CXL stack — no custom driver; MCTP / PLDM / Redfish management

SPECIFICATIONS

Host link	PCIe Gen5 ×16 / CXL 3.0 Type 3; ×16, 2××8, 4××4; SRIS
Memory	4 ch DDR4-3200 (72-bit, 2 DPC, RDIMM) or LPDDR4 / 4X-4266; up to 1 TB
Cache	8 MB, MII-managed allocation
Intelligence	Memory AI Agent (L3): 5 modes — Observe, Advise, Shadow, Autonomous, Fail-safe
Rails	VDD 0.8 V · VDDQ 1.2 / 1.1 / 0.6 V by mode · SERDES 0.8 + 1.5 / 1.8 V
Package	FCBGA 45 × 45 mm, 1,936 balls, 1.0 mm pitch
Samples	ES 3Q 2027 · QS 1Q 2028 · MP 3Q 2028

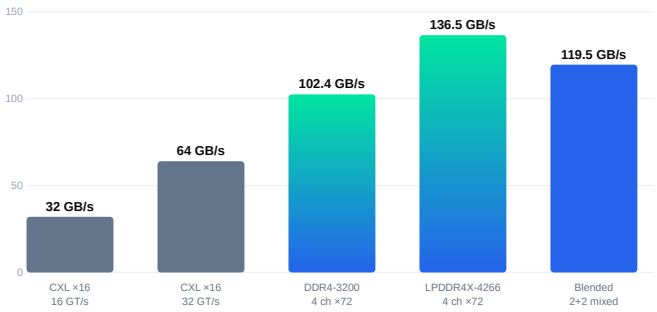
ARCHITECTURE

A CXL Type 3 controller between your hosts and your DRAM.



Host side: PCIe-5 PIPE PHY + CXL 3.0 controller. Memory side: MEMTECH combo DDR4 / LPDDR4X controller + PHY (×4 channels), RISC-V management, MII engine.

MEMORY BANDWIDTH WHERE IT COUNTS



Four DDR4-3200 channels (102 GB/s aggregate) saturate a ×16 CXL link at 16 GT/s and scale with the 32 GT/s PHY option.

VALIDATED LIKE A MEMORY COMPANY VALIDATES

- SERDES: EyeSurf eye capture, PRBS 7–31, loopbacks, ATE at-speed vectors
- DDR PHY: per-bit margin maps exported as MII telemetry; 65-corner sign-off plan
- Compliance: PCI-SIG, CXL Type 3 device interop matrix
- Reliability: ESD 2 kV HBM / 250 V CDM · EM 10-yr @ 110 °C · HTOL 1,000 h

DEPLOYMENT MODELS

Capacity tier — 1 TB volatile expansion per device; DAX or kmem onlining

Pooling without a switch — 4 hosts × ×4, per-host HDM partitions, QoS arbitration

AI serving — KV-cache and embedding store behind the GPU node

Second-life DDR4 — redeploy qualified DDR4 fleets behind modern CXL hosts

CO-DESIGN DELIVERABLES

- Per-net pin-delay table (RDL + package) for PCB skew compensation
- HFSS package model per byte + PowerSI PDN model (Touchstone / SPICE)
- IBIS 7.x power-aware models; SI/PI sign-off plan (HFSS + PowerSI), 3–5 weeks / family
- Reference 6-layer PCB rules — DDR4-3200 closes with +76 ps margin, no HDI

MEMTECH — **California Memory Technologies, Inc.** Founded 2020, Cupertino CA. Silicon Catalyst graduate; veterans of NVIDIA, Intel and Marvell. Differentiated by **MII** (Memory Intelligence Infrastructure), **Yield Improvement services** and **DDR Test Solutions**.

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